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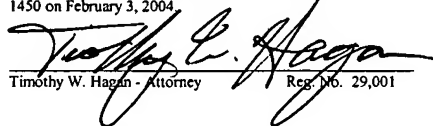
Application of

Applicants : Tran et al.
Serial No. : 10/705,707
Filed : November 11, 2003
Title : **TRENCH BURIED BIT LINE MEMORY DEVICES AND METHODS
THEREOF**
Docket : MIO 0100 VA/40509.274/01-1043.01

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

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Timothy W. Hagan - Attorney Reg. No. 29,001

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UNDER 37 CFR §§ 1.56, 1.97, AND 1.98

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This Information Disclosure Statement is being filed within the period set forth in 37 CFR §1.97(b) because it is filed within three months of the filing date of a national application or within three months of the date of entry of the national stage as set forth in 37 CFR §1.491 in an international application.

Serial No. 10/705,707

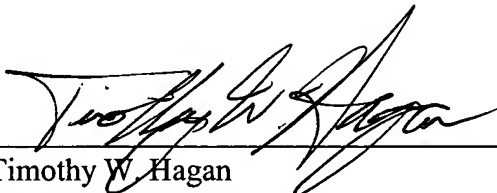
Docket No. MIO 0100 VA/40509.274/01-1043.01

This Information Disclosure Statement is being filed within the period set forth in 37 CFR §1.97(b) because it is believed to be filed before the mailing date of a first office action on the merits.

The Office has waived the requirement pursuant to 37 CFR 1.98 (a)(2)(i) for submitting a copy of each cited U.S. patent and each U.S. patent application publication for all U.S. national patent applications filed after June 30, 2003 and for all international applications that have entered the national stage under 35 USC § 371 after June 30, 2003. Therefore, no copies of each cited U.S. patent and each cited U.S. patent application publication are enclosed, but the cited U.S. patents and the cited U.S. patent application publications are listed on PTO/SB/08A.

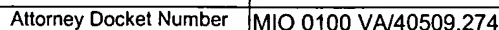
Respectfully submitted,
DINSMORE & SHOHL LLP

By


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